1st IEEE International Workshop on

CHIPLET INTERCONNECT TEST and REPAIR

in conjunction with IEEE European Test Symposium 2024
Thursday, May 23, 16:00-18:30h and Friday, May 24, 08:30-16:00h, 2024
https://ets24.nl/index.php/workshops/citar/

Call for Submissions

The first IEEE International Workshop on Chiplet Interconnect Test and Repair (CITaR) focuses exclusively on the test and repair of interconnects for chiplet-based, three-dimensional stacked ICs, and the on-chip infrastructure which enables that. These ICs include so-called 2.5D-, 3D-, and 5.5D-stacked ICs. Die-to-die interconnects might contain micro-bump pairs, hybrid bonds, interposer wires, and through-silicon vias (TSVs). While these stacked ICs offer many attractive advantages with respect to heterogeneous integration, small form-factor, high bandwidth and performance, and low power dissipation, there are many open issues with respect to testing and repairing their inter-die interconnects. The CITaR Workshop offers a unique forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

The CITaR Workshop will take place in conjunction with the IEEE European Test Symposium (ETS) in the Marriott Hotel in The Hague in the Netherlands and is technically sponsored by the Test Technology Technical Council (TTTC) of IEEE Computer Society.

Topic Areas – You are invited to participate and submit your technical work in this domain to the CITaR Workshop. The workshop's areas of interest include (but are not limited to) the following topics:

- Built-In-Self-Test (and Repair) for Chiplet Interconnects
- Defects in Chiplet Interconnects
- Design-for-Test for and Repair of Chiplet Interconnects
- DfT Architectures for Chiplet-Based ICs
- EDA Design-to-Test Flow for Chiplet Interconnects
- Failure Analysis for Chiplet Interconnects
- Fault-Tolerant Design for Chiplet Interconnects
- Interposer Testing
- Mid- and Post-Bond Testing
- Open Interfaces between Chiplets
- Reliability of Chiplet Interconnects
- Security and Chiplet Interconnects
- Standards for Chiplet Interconnects, incl. UCIe, AIB, etc.
- Standards for Chiplet Interconnect Test and Repair, incl. P3405
- Standards for Chiplet Testing, incl. IEEE Std 1838™
- Test Flow Optimization for Chiplet Interconnects
- Test Pattern Generation for Chiplet Interconnects
- Yield of Stacked Dies and their Interconnects

Submission Instructions – Submissions must be sent in as PDF files. The workshop prefers full paper submissions (of up to six pages), but also allows (extended) abstract submissions. Detailed submission instructions can be found at the workshop's website: https://ets24.nl/index.php/workshops/citar/. All submissions will be subject to selection with as evaluation criteria their suitability for the workshop, originality, technical soundness, and presented results. Submissions can be selected either for oral presentation ("papers") or for poster presentation ("posters").

Publications – CITaR focuses on early information sharing and open and free discussions; therefore, the workshop will not publish formal proceedings. Instead, the workshop will make available to all its registered participants an electronic workshop digest (EWD), which includes all material that authors/presenters are willing to contribute in PDF format: abstract, paper, slides, posters, background material, etc. This allows speakers to submit their workshop paper to a formal (IEEE or otherwise) conference and/or journal, leveraging the audience feedback and discussions on their early presentation at the CITaR Workshop.

Key Dates & Deadlines

- Submission deadline : ~~March 4, 2024 (23:59h AoE)~~ March 25, 2024
- Notification of acceptance : ~~March 11, 2024~~ April 1, 2024
- Author registration deadline: ~~March 15, 2024~~
  (Discount registration deadline: April 15, 2024)
- Camera-ready material : May 5, 2024 (23:59h AoE)

Further Information

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